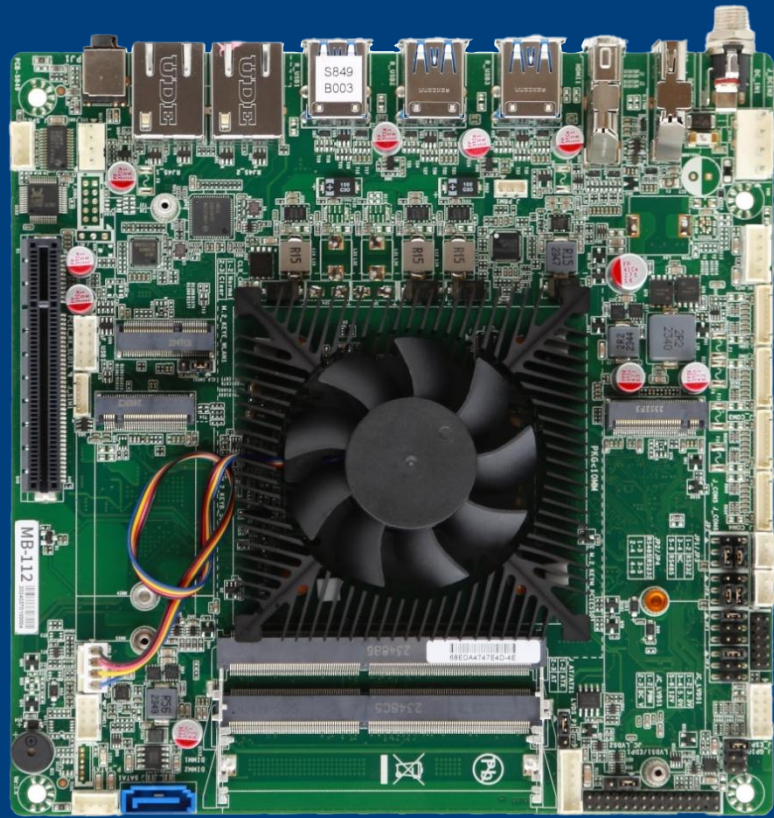


User Manual



Aicotek Motherboard | MB-112 User Manual

AICOTEK

Empowering the world with AI solutions

Contents

1. Models and Attentions	2
1.1 Models	2
1.2 Attentions	2
2. Specification	3
3. Functional Block Diagram	8
4. Mechanical Drawing	9
5. Jumpers / Headers and Connectors	10
6. Definition of Jumpers /Headers and Connectors	13
1) Mark No.4	13
J_DCIN3 (DC 12V Power Input Wafer 4*1 Pin 3.96 mm)	13
J_DCIN1 (DC 12V ATX 4P Power Input Connector)	13
2) Mark No.5 DC_OUT1 (DC 12V+5V Power Output Wafer 4*1 Pin 2.50 mm)	13
3) Mark No.6 LVDS1/EDP1 (LVDS/EDP Signal Header 15*2 Pin 2.00mm)	13
4) Mark No.7 LVDS_P1 (LVDS Backlight Control Wafer 6*1 Pin 2.00 mm)	14
5) Mark No.8 JC_LVDS1 (LVDS VDD Select Jumper 3*2 Pin 2.54 mm)	14
6) Mark No.9 JC_LVDS2 (LVDS Backlight PWM/CCFL Select Jumper 3*1 Pin 2.54 mm)	14
7) Mark No.13 J_SPK1 (Amplifier Wafer 4*1 Pin 2.00 mm)	15
8) Mark No.15 P_SATA1 (SATA Power Wafer 4*1 Pin 2.00 mm)	15
9) Mark No.19 J_SIM1 (SIM Card Wafer 6*1 Pin 1.25 mm)	15
10) Mark No.21 RJ45_1 (GbE LAN RJ45 Connector1)	15
11) Mark No.22 RJ45_2 (GbE LAN RJ45 Connector2)	16
12) Mark No.26 F_USB1 (Front USB2.0 Wafer1 5*2 Pin 2.00 mm)	16
13) Mark No.27 F_USB2 (Front USB2.0 Wafer2 5*2 Pin 2.00 mm)	16
14) Mark No.28 J_COM1 (COM1 Wafer 9*1 Pin 1.25 mm)	17
15) Mark No. 29 J_COM2 (COM2 Wafer 9*1 Pin 1.25 mm)	17
16) Mark No.30 J_COM3 (COM3 Wafer 9*1 Pin 1.25 mm)	17
17) Mark No. 31 J_COM4 (COM4 Wafer 9*1 Pin 1.25 mm)	18
18) Mark No.32 J_COM5 (COM5 Wafer 3*1 Pin 2.00 mm)	18
19) Mark No.33/34 JP1/JP2 (COM5 RS232/RS485 Select Jumper1 3*2 Pin 2.54mm)	18
20) Mark No. 35 J_COM6 (COM6 Wafer 3*1 Pin 2.00 mm)	18
21) Mark No.36/37 JP3/JP4 (COM6 RS232/RS485 Select Jumper2 3*2 Pin 2.54mm)	19
22) Mark No.38 J_GPIO1 (GPIO Wafer 5*2 Pin 2.00 mm)	19
23) Mark No.39 J_TCH1 (I2C Touch Screen Wafer 6*1 Pin 1.25 mm)	19
24) Mark No.40 F_PANEL1 (Front Panel Wafer 4*2 Pin 2.00 mm)	19
25) Mark No.41 CPU_FAN1 (CPU FAN Wafer 4*1 Pin 2.54 mm)	20
26) Mark No.42 SYS_FAN1 (System FAN Wafer 4*1 Pin 2.54 mm)	20
27) Mark No.43 AT/ATX1 (AT or ATX Select Jumper 3*1 Pin 2.54 mm)	20
28) Mark No.44 CLR_CMOS1 (CMOS Clear Jumper 3*1 Pin 2.54 mm)	20
29) Mark No.45 J_ME1 (ME Flash Jumper 3*1 Pin 2.54 mm)	20
30) Mark No.46 J_BAT1 (CMOS Battery Wafer 2*1 Pin 1.25 mm)	20
31) Mark No.47 J_ESPI1 (ESPI debug Header 6*2 Pin 2.00 mm)	21

1. Models and Attentions

1.1 Models

This manual is applied to following models:

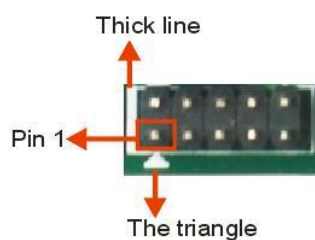
Model	CPU	COM	LAN	HDMI	LVDS/ EDP	DP++	USB	M.2 B-Key	M.2 M-KEY	M.2 E-KEY	SATA 3.0
MB-112-1215U	i3-1215U	6	2	1	LVDS	1	8	PCIe+ USB2.0	PCIe x4	PCIe+ USB2.0	1
MB-112-1235U	i5-1235U	6	2	1	LVDS	1	8	PCIe+ USB2.0	PCIe x4	PCIe+ USB2.0	1
MB-112-1255U	i7-1255U	6	2	1	LVDS	1	8	PCIe+ USB2.0	PCIe x4	PCIe+ USB2.0	1
MB-112-1315U	i3-1315U	6	2	1	LVDS	1	8	PCIe+ USB2.0	PCIe x4	PCIe+ USB2.0	1
MB-112-1335U	i5-1335U	6	2	1	LVDS	1	8	PCIe+ USB2.0	PCIe x4	PCIe+ USB2.0	1
MB-112-1355U	i7-1355U	6	2	1	LVDS	1	8	PCIe+ USB2.0	PCIe x4	PCIe+ USB2.0	1

1.2 Attentions

1) Notes under a table or figure indicate the difference of models, or alternative definition of specific pin of the header (jumper/connector).

2) How to identify the first pin of a header or jumper

- Usually, there is a thick line or a triangle near the header's or jumper's pin 1.



- Square pad, which you can find on the back of the motherboard, is usually used for pin 1.



2.Specification

Model		MB-112-1215U	MB-112-1235U	MB-112-1255U
CPU	CPU Model	Intel® Core™ Alder Lake-P Processor		
		i3-1215U	i5-1235U	i7-1255U
	Clock Speed	1.20GHz	1.30GHz	1.70GHz
	Multi-Core	6	10	10
	TDP	15W	15W	15W
	Graphics	Intel® UHD Graphics	Intel® Iris® Xe Graphics	
		up to 64 EUs, 1.10 GHz	up to 80 EUs, 1.20 GHz	up to 96 EUs, 1.25 GHz
Display		1 * HDMI(TYPE-A): max resolution up to 4096*2304@30Hz 1 * LVDS1/EDP1(Header): LVDS max 1920*1080 Dual channel 24-bits or EDP max 3840*2160@60Hz (Default LVDS) 1 * DP (TYPE-A): max resolution up to 4096*2304@60Hz		
Memory		2 * Support DDR4 3200 MHz, 2 * non-ECC SO-DIMM Slot, up to 2*32GB		
Storage		1 * SATA3.0 7P Connector (with 1 * SATA Power Wafer) 1 * M.2 M-Key Slot (PCIE x4/SATA, Support PCIE Gen3 x4 NVMe/SATA SSD, Auto Detect, 2280)		
Ethernet		1 * Intel® i210AT GbE LAN Chip (RJ45,10/100/1000 Mbps)		
		1 * Intel® i219-V GbE LAN Chip (RJ45, 10/100/1000 Mbps)	1 * Intel® i219-LM GbE LAN Chip (RJ45,10/100/1000 Mbps)	
Audio		Realtek Audio HDA Codec, 1 * Line-Out + MIC 2in1 3.5mm Jack (Default CTIA, OMTP optional) 1 * R/L Amplifier Wafer, 3-W (per channel) into an 8- Ω Loads		
Expansion Slots		1 * PCI-E 8x Slot (PCIE Gen4 x4 signal) 1 * M.2 B-Key Slot (PCIE + USB3.0 + USB2.0, Default PCIE + USB2.0, Support 5G/4G, 3042/3052) ^{[1][2]} 1 * M.2 E-Key Slot (PCIE+USB2.0, Support WIFI+BT, 2230) ^[3] 1 * SIM Card Wafer		
COM		4 * RS232 (COM1-4, Wafer, Full Lanes) 2 * RS232/RS485 (COM5-6, Wafer, Two Lanes)		
USB ^{[2][3]}		6 * USB3.0 (TYPE-A, Rear IO) ^[1] 2 * USB2.0 (Wafer, Internal)		
Other Ports		1 * 8-bit GPIO Header 1 * ESPI Header 1 * Front Panel Wafer 1 * CPU FAN Wafer 1 * System FAN Wafer 1 * Power Debug Wafer 1 * AT or ATX Select Jumper 1 * CMOS Clear Jumper 1 * CMOS Battery Wafer		
System		Windows 10 IoT Enterprise 2021 LTSC, Windows 10 (21H2), Windows 11 (21H2) or later, Linux Kernel 5.17 or later		

Temperature	Storage: -20~75°C Operating: 0~60°C
BIOS	AMI UEFI BIOS (Support Watchdog Timer)
Power Supply	DC12V (DC24V BOM Optional) 1 * DC 12V Power Input Thread Connector (Mini-Din 4P Jack Optional) 1 * DC 12 Power Input Wafer (ATX 4P Optional) 1 * DC 12V+5V Power Output Wafer
Factor	170mm*170mm

Notes:

[1]: USB3.0 signal of M.2_KEYB_SSD/WWAN1 colay with R_USB2_UP. (BOM selectable) They could not be used at the same time.

[2]: USB2.0 signal of M.2_KEYB_SSD/WWAN1 colay with one of USB2.0 signal for F_USB2. They could not be used at the same time.

[3]: USB2.0 signal of M.2_KEYE_WLAN1 colay with one of USB2.0 signal for F_USB2. They could not be used at the same time.

Model		MB-112-1315U	MB-112-1335U	MB-112-1355U
CPU	CPU Model	Intel® Core™ Raptor Lake-P Processor		
		i3-1315U	i5-1335U	i7-1355U
	Clock Speed	1.2 GHz	1.3 GHz	1.70GHz
	Multi-Core	2P4E	2P8E	2P8E
	TDP	15W	15W	15W
	Graphics	Intel® UHD Graphics	Intel® Iris® Xe Graphics	
		Up to 64 EUs, 1.25 GHz	Up to 80 Eus, 1.25 GHz	up to 96 EUs, 1.25 GHz
Display		1 * HDMI(TYPE-A): max resolution up to 4096*2304@30Hz 1 * LVDS1/EDP1(Header): LVDS max 1920*1080 Dual channel 24-bits or EDP max 3840*2160@60Hz (Default LVDS) 1 * DP (TYPE-A): max resolution up to 4096*2304@60Hz		
Memory		2 * Support DDR4 3200 MHz, 2 * non-ECC SO-DIMM Slot, up to 2*32GB		
Storage		1 * SATA3.0 7P Connector (with 1 * SATA Power Wafer) 1 * M.2 M-Key Slot (PCIe x4/SATA, Support PCIe Gen3 x4 NVMe/SATA SSD, Auto Detect, 2280)		
Ethernet		1 * Intel® i210AT GbE LAN Chip (RJ45,10/100/1000 Mbps)		
		1 * Intel® i219-V GbE LAN Chip (RJ45, 10/100/1000 Mbps)	1 * Intel® i219-LM GbE LAN Chip (RJ45,10/100/1000 Mbps)	
Audio		Realtek Audio HDA Codec, 1 * Line-Out + MIC 2in1 3.5mm Jack (Default CTIA, OMTP optional) 1 * R/L Amplifier Wafer, 3-W (per channel) into an 8- Ω Loads		
Expansion Slots		1 * PCI-E 8x Slot (PCIe Gen4 x4 signal) 1 * M.2 B-Key Slot (PCIe + USB3.0 + USB2.0, Default PCIe + USB2.0, Support 5G/4G, 3042/3052) ^{[1][2]} 1 * M.2 E-Key Slot (PCIe+USB2.0, Support WIFI+BT, 2230) ^[3] 1 * SIM Card Wafer		
COM		4 * RS232 (COM1-4, Wafer, Full Lanes) 2 * RS232/RS485 (COM5-6, Wafer, Two Lanes)		
USB ^{[2][3]}		6 * USB3.0 (TYPE-A, Rear IO) ^[1] 2 * USB2.0 (Wafer, Internal)		
Other Ports		1 * 8-bit GPIO Header 1 * ESPI Header 1 * Front Panel Wafer 1 * CPU FAN Wafer 1 * System FAN Wafer 1 * Power Debug Wafer 1 * AT or ATX Select Jumper 1 * CMOS Clear Jumper 1 * CMOS Battery Wafer		
System		Windows 10 IoT Enterprise 2021 LTSC, Windows 10 (21H2), Windows 11 (21H2) or later, Linux Kernel 5.17 or later		
Temperature		Storage: -20~75℃ Operating: 0~60℃		

BIOS	AMI UEFI BIOS (Support Watchdog Timer)
Power Supply	DC12V (DC24V BOM Optional) 1 * DC 12V Power Input Thread Connector (Mini-Din 4P Jack Optional) 1 * DC 12 Power Input Wafer (ATX 4P Optional) 1 * DC 12V+5V Power Output Wafer
Factor	170mm*170mm

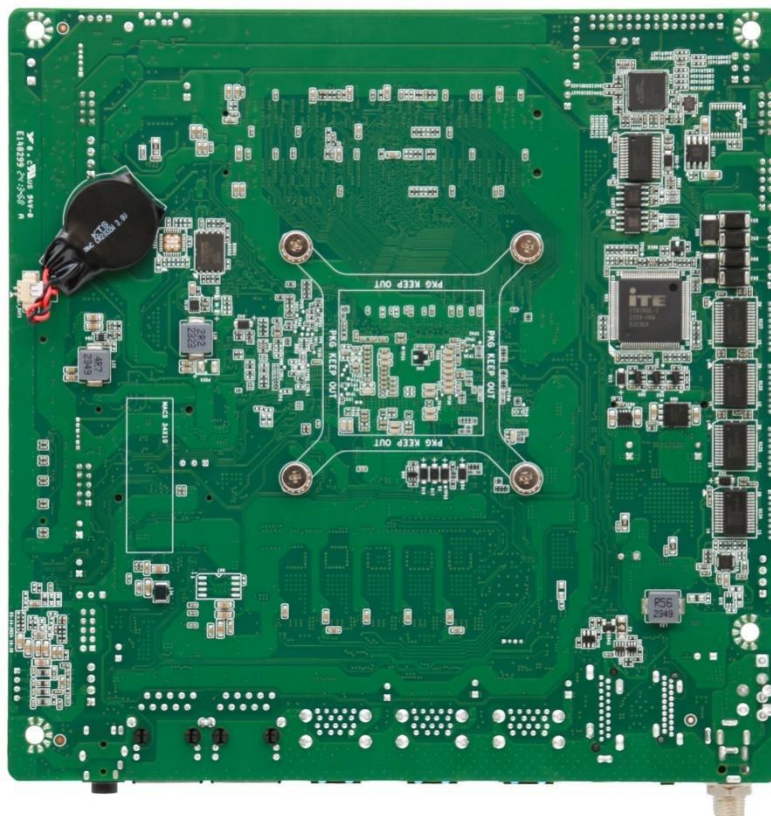
Notes:

[1]: USB3.0 signal of M.2_KEYB_SSD/WWAN1 colay with R_USB2_UP. (BOM selectable) They could not be used at the same time.

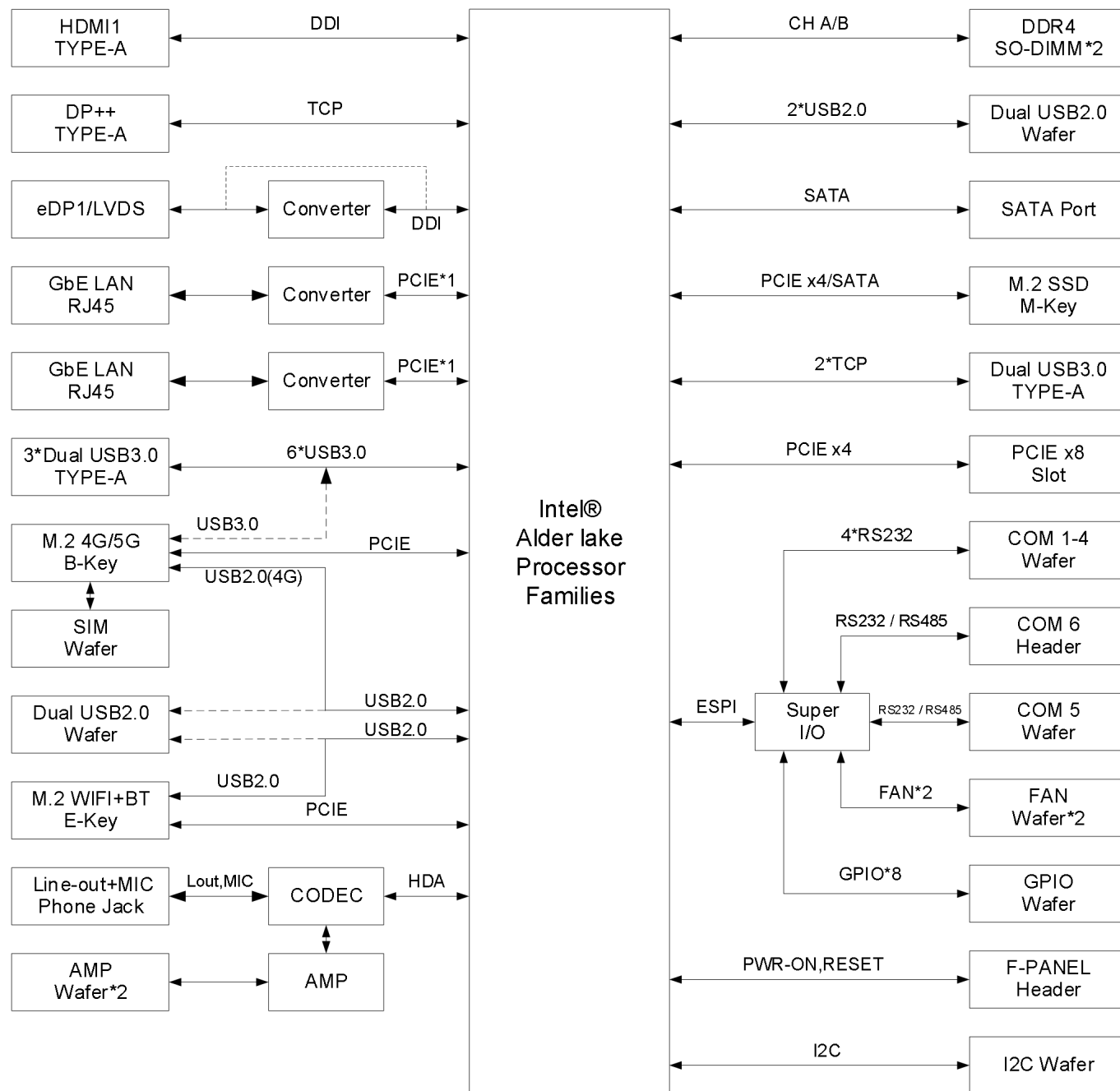
[2]: USB2.0 signal of M.2_KEYB_SSD/WWAN1 colay with one of USB2.0 signal for F_USB2. They could not be used at the same time.

[3]: USB2.0 signal of M.2_KEYE_WLAN1 colay with one of USB2.0 signal for F_USB2. They could not be used at the same time.

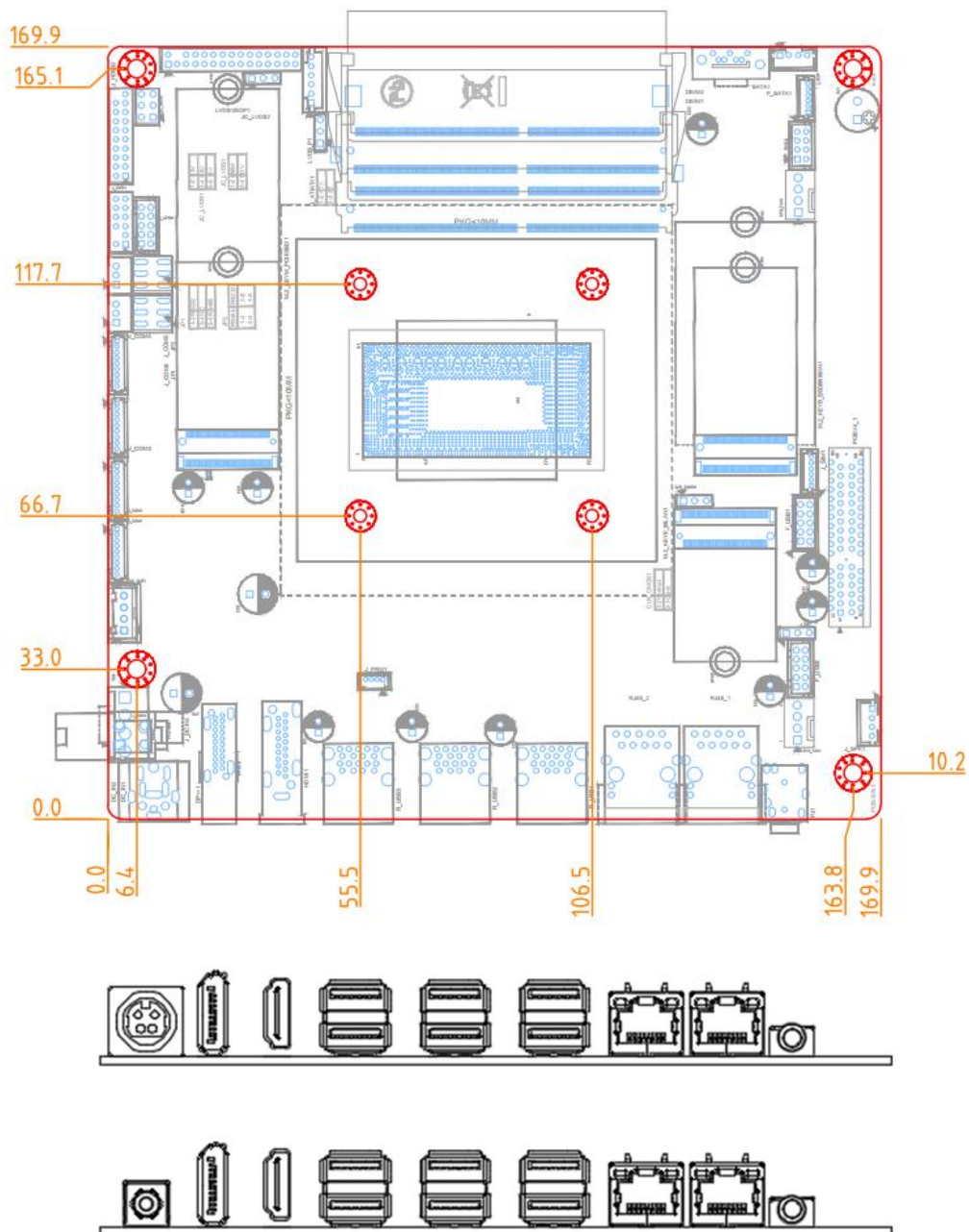




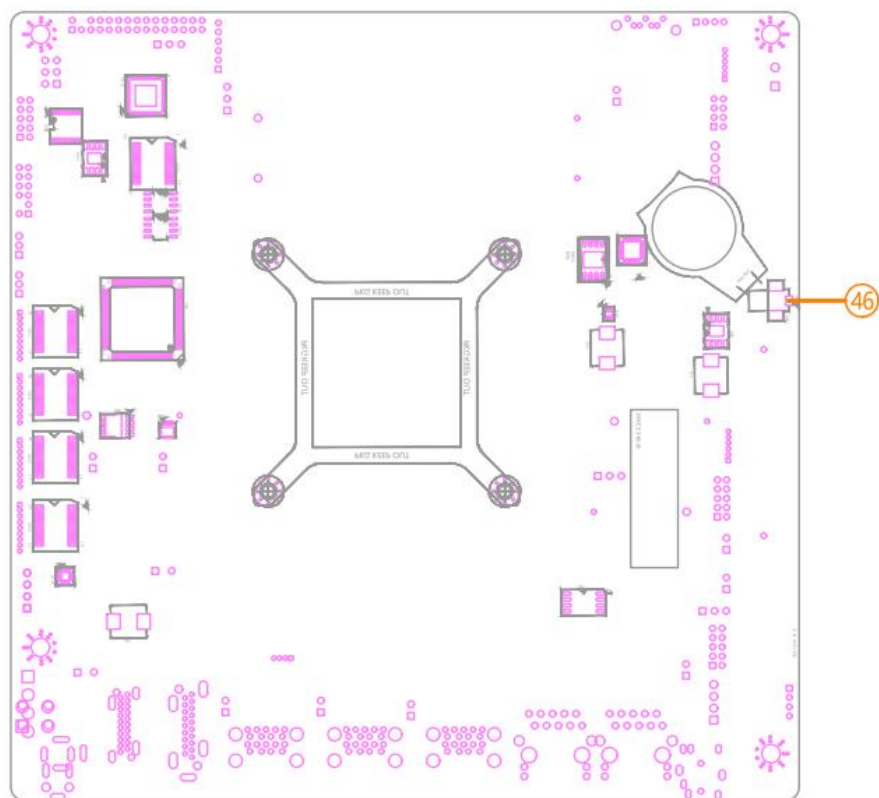
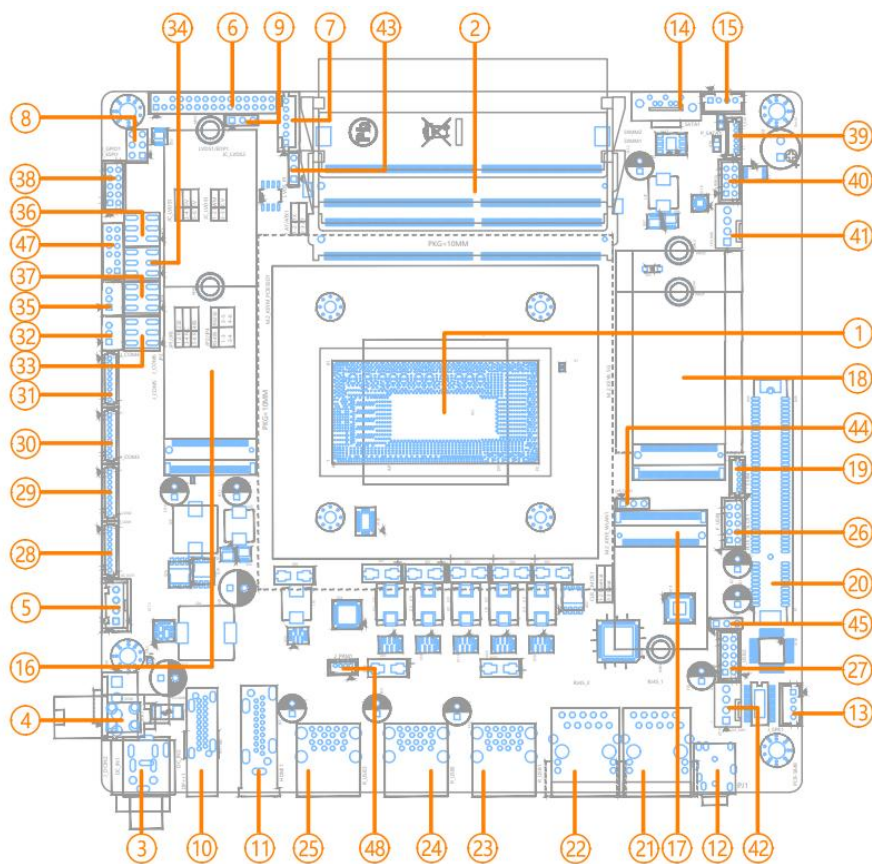
3.Functional Block Diagram



4.Mechanical Drawing



5. Jumpers / Headers and Connectors



Jumpers / Headers and Connectors

①	U1	CPU
②	DIMM1-2	DDR4 SO-DIMM Slot1/2
③	DC_IN1 (DC_IN2)	DC 12V Power Input Thread Connector (DC 12V Power Input Mini-DIN 4P Jack)
④	J_DCIN3 (J_DCIN2)	DC 12V Power Input Wafer (DC 12V ATX 4P Power Input Connector)
⑤	DC_OUT1	DC 12V+5V Power Output Wafer
⑥	LVDS1/EDP1	LVDS/eDP Signal Header
⑦	LVDS_P1	LVDS Backlight Control Wafer
⑧	JC_LVDS1	LVDS VDD Select Jumper
⑨	JC_LVDS2	LVDS Backlight PWM/CCFL Select Jumper
⑩	DP++1	DP upright Connector
⑪	HDMI1	HDMI upright TYPE-A Connector
⑫	PJ1	Line-Out + MIC 2in1 3.5mm Jack
⑬	J_SPK1	Amplifier Wafer
⑭	SATA1	SATA3.0 7P Connector
⑮	P_SATA1	SATA Power Wafer
⑯	M.2_KEYM_PCIESSD1	M.2 M-Key Slot (PCIe x4, Support NVMe PCIe Gen4 x4/ SATA SSD, 2242/2280)
⑰	M.2_KEYE_WLAN1	M.2 E-Key Slot (PCIe+USB2.0, Support WIFI+BT, 2230)
⑱	M.2_KEYB_5G	M.2 B-Key Slot (PCIe/USB3.0 + USB2.0, Support 4G/5G, 2242/3052)
⑲	J_SIM1	SIM Card Wafer
⑳	PCIE_8X_SLOT1	PCI-E 8x Slot (PCIe x4 Signal)
㉑	RJ45_1	GbE LAN RJ45 Connector1
㉒	RJ45_2	GbE LAN RJ45 Connector2
㉓	R_USB1	Dual USB3.0 TYPE-A Connector1
㉔	R_USB2	Dual USB3.0 TYPE-A Connector2
㉕	R_USB3	Dual USB3.0 TYPE-A Connector3
㉖	F_USB1	Front Dual-USB2.0 Wafer1
㉗	F_USB2	Front Dual-USB2.0 Wafer2
㉘	J_COM1	COM1 Wafer
㉙	J_COM2	COM2 Wafer
㉚	J_COM3	COM3 Wafer
㉛	J_COM4	COM4 Wafer
㉜	J_COM5	COM5 Wafer
㉝	JP1	COM5 RS232/RS485 Select Jumper1
㉞	JP2	COM5 RS232/RS485 Select Jumper2
㉟	J_COM6	COM6 Wafer
㊱	JP3	COM6 RS232/RS485 Select Jumper1
㊲	JP4	COM6 RS232/RS485 Select Jumper2

③⑧	J_GPIO1	GPIO Wafer
③⑨	J_TCH1	I2C Touch Screen Wafer
④⑩	F_PANEL1	Front Panel Wafer
④①	CPU_FAN1	CPU FAN Wafer
④②	SYS_FAN1	System FAN Wafer
④③	AT/ATX1	AT or ATX Select Jumper
④④	CLR_CMOS1	CMOS Clear Jumper
④⑤	J_ME1	ME Flash Jumper
④⑥	J_BAT1	CMOS Battery Wafer
④⑦	J_ESPI1	ESPI Debug Header
④⑧	J_PRM1	Power Debug Wafer

6. Definition of Jumpers /Headers and Connectors

1) Mark No.4

J_DCIN3 (DC 12V Power Input Wafer 4*1 Pin 3.96 mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCC_IN	3	GND
	2	VCC_IN	4	GND

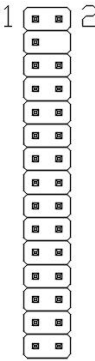
J_DCIN1 (DC 12V ATX 4P Power Input Connector)

Graphic	Pin	Definition	Pin	Definition
	1	GND	3	VCC_IN
	2	GND	4	VCC_IN

2) Mark No.5 DC_OUT1 (DC 12V+5V Power Output Wafer 4*1 Pin 2.50 mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCC12	3	GND
	2	GND	4	VCC5

3) Mark No.6 LVDS1/EDP1 (LVDS/EDP Signal Header 15*2 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
	1	VDD_PANEL ^[1]	2	VDD_PANEL ^[1]
	3	VDD_PANEL ^[1]		
	5	EDP1_HPD/ LVDS_PRSENT#	6	EDP1_HPD/ LVDS_PRSENT#
	7	LVDS_A_DATA0-	8	LVDS_A_DATA0+
	9	LVDS_A_DATA1-	10	LVDS_A_DATA1+
	11	LVDS_A_DATA2-	12	LVDS_A_DATA2+
	13	GND	14	GND
	15	LVDS_A_CLK-	16	LVDS_A_CLK+
	17	LVDS_A_DATA3-	18	LVDS_A_DATA3+
	19	LVDS_B_DATA0- EDP1_TX0- ^[2]	20	LVDS_B_DATA0+ EDP1_TX0+ ^[2]
	21	LVDS_B_DATA1- EDP1_TX1- ^[2]	22	LVDS_B_DATA1+ EDP1_TX1+ ^[2]

	23	LVDS_B_DATA2- EDP1_TX2- ^[2]	24	LVDS_B_DATA2+ EDP1_TX2+ ^[2]
	25	GND	26	GND
	27	LVDS_B_CLK- EDP1_TX3-	28	LVDS_B_CLK+ EDP1_TX3+ ^[2]
	29	LVDS_B_DATA3- EDP1_AUX- ^[2]	30	LVDS_B_DATA3+ EDP1_AUX+ ^[2]

Notes:

[1]: Panel Power VDD is 3.3V by default, 5V/12V is selectable by “LVDS VDD Select Jumper” (JC_LVDS1, Mark 8).

[2]: It supports LVDS by default and can support eDP if specified. (resistor selectable)

4) Mark No.7 LVDS_P1 (LVDS Backlight Control Wafer 6*1 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	GND	4	LVDS_BKLT_EN
	2	GND	5	VCC12
	3	LVDS_BKLT_CTL ^[1]	6	VCC12

Notes:

[1]: LVDS_BKLT can be controlled by PWM(Default) /CCFL, selectable by “LVDS Backlight PWM/CCFL Select Jumper” (JC_LVDS2, Mark 9).

5) Mark No.8 JC_LVDS1 (LVDS VDD Select Jumper 3*2 Pin 2.54 mm)

Graphic	Setting	Function
	1-2(Default)	VCC3.3
	3-4	VCC5
	5-6	VCC12

6) Mark No.9 JC_LVDS2 (LVDS Backlight PWM/CCFL Select Jumper 3*1 Pin 2.54 mm)

Graphic	Setting	Function
	1-2(Default)	Controlled by PWM
	2-3	Controlled by CCFL ^[1]

Notes:

[1]: Controlled by CCFL by default, PWM# optional. (resistor selectable)

7) Mark No.13 J_SPK1 (Amplifier Wafer 4*1 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	SPK_OUT_L-	3	SPK_OUT_R-
	2	SPK_OUT_L+	4	SPK_OUT_R+

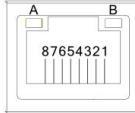
8) Mark No.15 P_SATA1 (SATA Power Wafer 4*1 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCC12	3	GND
	2	GND	4	VCC5

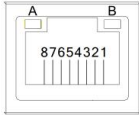
9) Mark No.19 J_SIM1 (SIM Card Wafer 6*1 Pin 1.25 mm)

Graphic	Pin	Definition	Pin	Definition
	1	PWR	4	CLK
	2	DATA	5	RESET
	3	GND	6	VPP

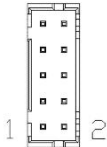
10) Mark No.21 RJ45_1 (GbE LAN RJ45 Connector1)

Graphic	Pin	Definition		Pin	Definition	
	1	MDI0+		5	MDI2-	
	2	MDI0-		6	MDI1-	
	3	MDI1+		7	MDI3+	
	4	MDI2+		8	MDI3-	
	A	Active LED	ACT: Twinkling Yellow	B	Speed LED	1000M: Turn Orange
			Only LINK: Lights On			100M: Turn Green
			Stop: Lights Off			10M: Lights Off

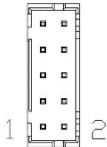
11) Mark No.22 RJ45_2 (GbE LAN RJ45 Connector2)

Graphic	Pin	Definition		Pin	Definition	
	1	MDI0+		5	MDI2-	
	2	MDI0-		6	MDI1-	
	3	MDI1+		7	MDI3+	
	4	MDI2+		8	MDI3-	
	A	Active LED	ACT: Twinkling Yellow	B	Speed LED	1000M: Turn Orange
			Only LINK: Lights On			100M: Turn Green
			Stop: Lights Off			10M: Lights Off

12) Mark No.26 F_USB1 (Front USB2.0 Wafer1 5*2 Pin 2.00 mm)

Graphic	Pin	Definition		Pin	Definition	
	2	VCC5		1	VCC5	
	4	USB2.0_2-		3	USB2.0_1-	
	6	USB2.0_2+		5	USB2.0_1+	
	8	GND		7	GND	
	10	GND		9	GND	

13) Mark No.27 F_USB2 (Front USB2.0 Wafer2 5*2 Pin 2.00 mm)

Graphic	Pin	Definition		Pin	Definition	
	2	VCC5		1	VCC5	
	4	USB2.0_2-		3	USB2.0_1-	
	6	USB2.0_2+		5	USB2.0_1+	
	8	GND		7	GND	
	10	GND		9	GND	

14) Mark No.28 J_COM1 (COM1 Wafer 9*1 Pin 1.25 mm)

Graphic	Pin	Definition	Pin	Definition
	1	DCD/5V ^[1]	6	CTS
	2	DSR	7	DTR
	3	RXD	8	RI/12V ^[1]
	4	RTS	9	GND
	5	TXD		

Notes:

[1]: PIN1 of COM1 can be DCD# (default) /5V, selectable by resistor.

[2]: PIN8 of COM1 can be RI# (default) /12V, selectable by resistor.

15) Mark No. 29 J_COM2 (COM2 Wafer 9*1 Pin 1.25 mm)

Graphic	Pin	Definition	Pin	Definition
	1	DCD/5V ^[1]	6	CTS
	2	DSR	7	DTR
	3	RXD	8	RI/12V ^[1]
	4	RTS	9	GND
	5	TXD		

Notes:

[1]: PIN1 of COM2 can be DCD# (default) /5V, selectable by resistor.

[2]: PIN8 of COM2 can be RI# (default) /12V, selectable by resistor.

16) Mark No.30 J_COM3 (COM3 Wafer 9*1 Pin 1.25 mm)

Graphic	Pin	Definition	Pin	Definition
	1	DCD/5V ^[1]	6	CTS
	2	DSR	7	DTR
	3	RXD	8	RI/12V ^[1]
	4	RTS	9	GND
	5	TXD		

Notes:

[1]: PIN1 of COM2 can be DCD# (default) /5V, selectable by resistor.

[2]: PIN8 of COM2 can be RI# (default) /12V, selectable by resistor.

17) Mark No. 31 J_COM4 (COM4 Wafer 9*1 Pin 1.25 mm)

Graphic	Pin	Definition	Pin	Definition
	1	DCD/5V ^[1]	6	CTS
	2	DSR	7	DTR
	3	RXD	8	RI/12V ^[1]
	4	RTS	9	GND
	5	TXD		

Notes:

[1]: PIN1 of COM2 can be DCD# (default) /5V, selectable by resistor.

[2]: PIN8 of COM2 can be RI# (default) /12V, selectable by resistor.

18) Mark No.32 J_COM5 (COM5 Wafer 3*1 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	RXD/RS485+ ^[1]	3	GND
	2	TXD/RS485- ^[1]		

Notes:

[1]: J_COM5 can be selected by “COM5 RS232/RS485 Select Jumper1” (JP1/JP2, Mark 33/34).

19) Mark No.33/34 JP1/JP2 (COM5 RS232/RS485 Select Jumper1 3*2 Pin 2.54mm)

Graphic	Setting	Function
	JP1: 1-2 JP2: 3-5,4-6(Default)	RS232
	JP1: 5-6 JP2: 1-3,2-4	RS485

20) Mark No. 35 J_COM6 (COM6 Wafer 3*1 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	RXD/RS485+ ^[1]	3	GND
	2	TXD/RS485- ^[1]		

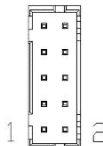
Notes:

[1]: J_COM6 can be selected by “COM6 RS232/RS485 Select Jumper2” (JP3/JP4, Mark 36/37).

21) Mark No.36/37 JP3/JP4 (COM6 RS232/RS485 Select Jumper 2 3*2 Pin 2.54mm)

Graphic	Setting	Function
	JP3: 1-2 JP4: 3-5,4-6(Default)	COM6: S232
	JP3: 5-6 JP4: 1-3,2-4	COM6: RS485

22) Mark No.38 J_GPIO1 (GPIO Wafer 5*2 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	2	SIO_GPO70 (0xA06 Bit0, H ^[1])	1	SIO_GPO71 (0xA06 Bit1, H ^[1])
	4	SIO_GPO72 (0xA06 Bit2, H ^[1])	3	SIO_GPO73 (0xA06 Bit3, H ^[1])
	6	SIO_GPI75 (0xA06 Bit5, H ^[1])	5	SIO_GPI74 (0xA06 Bit4, H ^[1])
	8	SIO_GPI77 (0xA06 Bit7, H ^[1])	7	SIO_GPI76 (0xA06 Bit6, H ^[1])
	10	+5V ^[2]	9	GND

Notes:

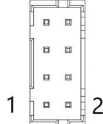
[1]: “H” or “L” means the default voltage is High or Low level (5V GPIO).

[2]: Power on this Pin is 5V by default, 3.3V is available if specified. (resistor selectable)

23) Mark No.39 J_TCH1 (I2C Touch Screen Wafer 6*1 Pin 1.25 mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCC3.3	4	TCH_RST_N
	2	GND	5	TCH_I2C_SCL
	3	TCH_INT_N	6	TCH_I2C_SDA

24) Mark No.40 F_PANEL1 (Front Panel Wafer 4*2 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	2	HDD_LED+	1	PWR_LED+
	4	HDD_LED-	3	PWR_LED-
	6	RESET-	5	PWR_ON+
	8	RESET+	7	PWR_ON-

25) Mark No.41 CPU_FAN1 (CPU FAN Wafer 4*1 Pin 2.54 mm)

Graphic	Pin	Definition	Pin	Definition
	1	GND	3	FAN Speed Detection
	2	VCC12	4	FAN Speed Control

26)Mark No.42 SYS_FAN1 (System FAN Wafer 4*1 Pin 2.54 mm)

Graphic	Pin	Definition	Pin	Definition
	1	GND	3	FAN Speed Detection
	2	VCC12	4	FAN Speed Control

27)Mark No.43 AT/ATX1 (AT or ATX Select Jumper 3*1 Pin 2.54 mm)

Graphic	Setting	Function
	1-2(Default)	ATX MODE
	2-3	AT MODE

28)Mark No.44 CLR_CMOS1 (CMOS Clear Jumper 3*1 Pin 2.54 mm)

Graphic	Setting	Function
	1-2(Default)	Normal
	2-3	Clear CMOS

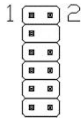
29)Mark No.45 J_ME1 (ME Flash Jumper 3*1 Pin 2.54 mm)

Graphic	Setting	Function
	1-2(Default)	Normal
	2-3	Debug

30)Mark No.46 J_BAT1 (CMOS Battery Wafer 2*1 Pin 1.25 mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCC_BAT	2	GND

31) Mark No.47 J_ESPI1 (ESPI debug Header 6*2 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	ESPI_IO0	2	VCC3.3
	3	ESPI_IO1		
	5	ESPI_IO2	6	ESPI_CLK
	7	ESPI_IO3	8	GND
	9	ESPI_CS0-	10	VCC3.3
	11	ESPI_ALERT0-	12	ESPI_RST0_N BUF_PLT_RST_N ^[1]

Notes:

[1]: Support BUF_PLT_RST_N by default, ESPI_RST0_N optional.

32) Mark No.48 J_PRM1 (Power Debug Wafer 4*1 Pin 1.25 mm)

Graphic	Pin	Definition	Pin	Definition
	1	GND	3	VCCIN_SCL
	2	IMVP_PE	4	VCCIN_SDA

【End】



Empowering the world with AI solutions

Baltesakker 17, 5625TC
Eindhoven, the Netherlands
www.aicotek.com
info@aicotek.com